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Goertzel block size N is like the number of points in an equivalent FFT. It controls the frequency resolution (also called bin width). ...

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Response of single FFT Bin - Uniform and Kaiser Windows. ... BAE Systems (formerly Plessey) and Thales (formerly EMI) in Europe, and has run a highly ...

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the FFT bin width, but does not change the ability to resolve two signals. ... The environmental and EMC testing were to be witnessed by the Army ...

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### 1 [A C-based RTL design verification methodology for complex microprocessor](#)



Joon-Seo Yim, Yoon-Ho Hwang, Chang-Jae Park, Hoon Choi, Woo-Seung Yang, Hun-Seung Oh, In-Cheol Park, Chong-Min Kyung

 June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**

Publisher: ACM Press

 Full text available: [pdf\(224.80 KB\)](#)

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As the complexity of high-performance microprocessor increases, functional verification becomes more and more difficult and RTL simulation emerges as the bottleneck of the design cycle. In this paper, we suggest C language-based design and verification methodology to enhance the simulation speed instead of the conventional HDL-based methodologies. RTL C model (StreC) describes the cycle-based behaviors of synchronous circuits and is followed by model refining and optimization using LifeTime Analyzer (LTA ...

### 2 [Verification of configurable processor cores](#)



Marínés Puig-Medina, Gülbin Ezer, Pavlos Konas

 June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

 Full text available: [pdf\(79.05 KB\)](#)

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This paper presents a verification methodology for configurable processor cores. The simulation-based approach uses directed diagnostics and pseudo-random program generators both of which are tailored to specific processor instances. A configurable and extensible test-bench serves as the framework for the verification process and offers components necessary for the complete SOC verification. Coverage analysis provides an evaluation of how well a specific design has been exercised, of the br ...

**Keywords:** co-simulation, configurable processor cores, coverage analysis, design verification, system-on-chip, test generation

### 3 [Testing: On automatic generation of RTL validation test benches using circuit testing techniques](#)



Indradeep Ghosh, Srivaths Ravi

 April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**